Remarks

Thorough examination by the Examiner is noted and appreciated.

The drawings have been amended and a proposed replacement sheet submitted to correct "24B" to "26B" in Figure 1F to make it consistent with Figure 1E and the Specification.

The Specification has been amended to correct grammatical errors.

The claims have been amended to clarify Applicants disclosed and claimed invention.

Support for the amendments is found in the original claims and the Specification.

No new matter has been added.

Claim Rejections under 35 USC 102(b)

Claims 1, 2, 5-9, 12, 13, and 16-19 stand rejected under 35 USC Section 102(b) as being anticipated by Leung et al. (US 6,468,855).

Leung et al. disclose a reduced topography DRAM cell that includes an access transistor and a storage capacitor (see Abstract). IN one embodiment, Leung et al. discloses a layout for the DRAM cell which "region 312 is laid out with minimum polysilicon gate spacing, which **is comparable to twice the size of the insulating sidewall spacers** 325". Leung et al. disclose "S/D doping and salicide are effectively excluded from region 312 without the need for additional processing steps."

Leung et al., however, does not disclose a process for forming the sidewall spacers, i.e., Leung et al. does not disclose first depositing a dielectric layer having a predetermined thickness and etching back the dielectric layer as Applicants have disclosed and claimed.

In addition, Leung et al., do not disclose or teach "wherein the predetermined distance is **less** than about twice the sidewall spacer width;" as Applicants disclose and claim.

In addition Leung et al. do not disclose an "**unetched** spacer dielectric layer portion overlying the first doped region" as Applicants have disclosed and claimed.

Thus, Leung et al. is insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Since Leung et al. fails to anticipate Applicants disclosed and claimed invention with respect to Applicants independent claims, neither does Hayashi anticipate Applicants dependent claims.

Claim Rejections under 35 USC 103(a)

1. Claims 10 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al., above.

Applicants reiterate the comments made above with respect to Leung et al.

Moreover, Leung et al. teach that the predetermined distance is **equal to** about twice the sidewall spacer width, i.e., "region 312 is laid out with minimum polysilicon gate spacing, which **is comparable to twice the size of the insulating sidewall spacers** 325". Leung et al. thereby **teach away** from Applicants disclosed and claimed invention.

In addition, as previously stated, nowhere do Leung et al. disclose or teach a method for forming the sidewall spacers. For example, the resulting structure shown formed in Figures 3E and 3F of Leung et al., shows **completely formed (etched)** sidewall spacers over the P- region, thereby teaching away from Applicants disclosed and claimed invention of an "**unetched spacer dielectric layer portion** overlying the

first doped region" as shown in Applicants Figures 1E and 1F (item 26B).

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

2. Claims 3, 11, 14, and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al., above, in view of Tzeng et al. (US 6, 670,664).

Statement of Common Ownership Pursuant to 35 USC 103(c)

Applicants attorney of record states that Tzeng et al. (US 6,670,664 B1, December 30, 2003) and Applicants instant application were, at the time the invention was made, owned by Taiwan Semiconductor Manufacturing Company. Therefore, Examiners use of Tzeng et al. as a reference in a 103(a) rejection appears to be improper under 35 USC §103(C).

However, while not agreeing Tzeng et al. may be properly be used as a reference in a rejection under 103(a), assuming *arguendo* that it is a properly used reference, Applicants respectfully traverse Examiner's rejection under 35 U.S.C. 103(a).

Tzeng et al. disclose an FET transistor laterally adjoining a metal oxide semiconductor capacitor device where a single fluorinated silicon oxide layer having a single thickness acts as both the gate dielectric layer for the FET transistor and as a capacitor dielectric layer for the capacitor device (see Abstract).

Tzeng also disclose completely formed sidewall spacers adjacent an FET transistor and adjacent a capacitor structure (e.g., see items 26c, 26d adjacent capacitors 24b and sidewalls 26e and 26f adjacent capacitor 24C. See also sidewalls

26g, 26h adjacent FET structure 24d and sidewalls 26i, 26j adjacent FET structure 24e. See discussion of Figure 6 at col 6, lines 42-58). Tzeng et al. discloses a completely different method to adjust the doping of the source/drain regions of the FET adjacent a capacitor structure (see e.g., col 6, lines 53-58).

Thus, Tzeng et al. disclose a structure significantly different from both Leung et al. and Applicants disclosed and claimed invention. Like Leung et al., Tzeng et al. discloses **completely formed sidewall spacers,** and does not disclose Applicants **unetched spacer dielectric layer portion overlying the first doped region,** thereby also teaching away from Applicants disclosed and claimed invention.

There is no apparent motivation to combine the teachings of Tzeng et al. and Leung et al. Nevertheless, even assuming *arguendo* a proper motivation for combining the teachings of Tzeng et al. and Leung et al., such combination does not produce Applicants disclosed and claimed invention.

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469*

U.S. 851 (1984).

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates

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Replacement Sheet
67,200-1178

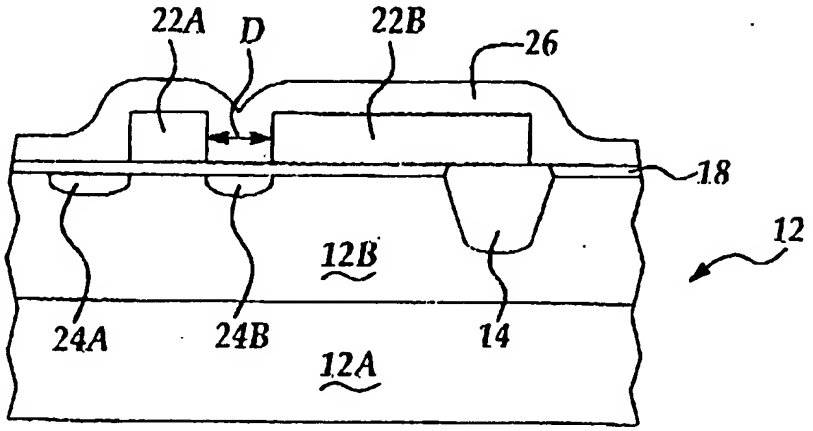

Figure 1D

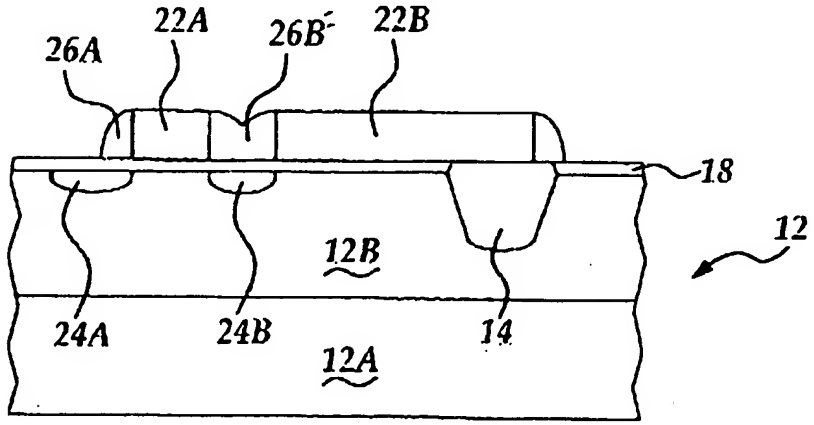

Figure 1E

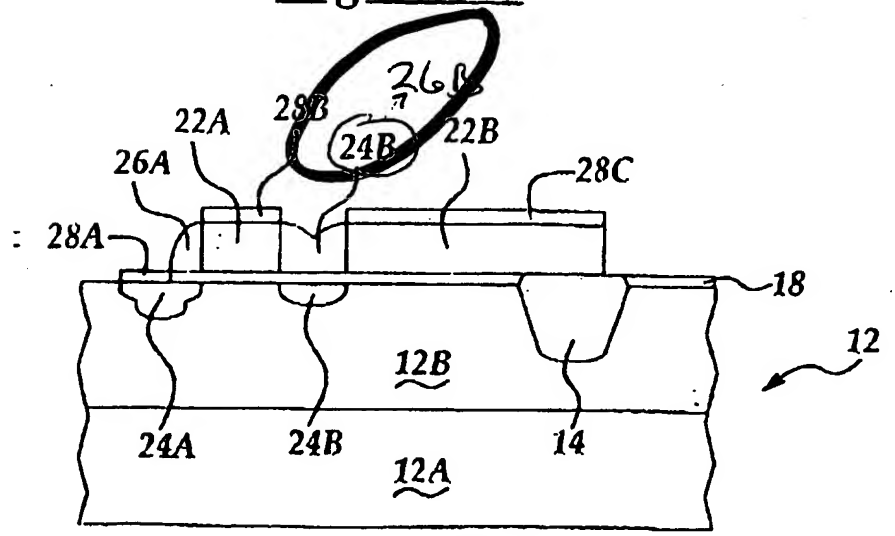

Figure 1F

Drawing Amendments

Please replace "24B" in Figure 1F, pointing to a dielectric portion between pass transistor 22A and storage capacitor 22B, with "26B" to make Figure 1F consistent with the Specification and with Figure 1E.